GaAs HBT PROFILE OPTIMIZATION USING THE TAGUCHI METHOD

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ABSTRACT

A method is presented for quantitatively optimizing HBT performance using a combination of physical and equivalent circuit models in the design-of-experiments framework. An optimized profile was designed which demonstrated over 4 dB improvement in *Gmax* at 10 GHz (over the M/A-COM baseline process) without resorting to reduced device dimensions and/or a thin base layer.

INTRODUCTION

An approach is presented for optimizing the heterojunction bipolar transistor (HBT) profile using Taguchi's Design of Experiments *(DoE)* method. This features a closed-loop design which combines physical modeling and equivalent circuit modeling to accurately predict the high-frequency performance of HBT's. This paper will discuss: (1) the *DoE* design approach, (2) the closed-loop modeling technique, and (3) the design validation. Further, the *DoE* method has been experimentally validated with three different HBT profiles.

This work differs from the conventional design approach where the effects of parameter changes can only be qualitatively described using analytical equations. It advances HBT device design technology by providing a systematic method to **quantitatively** investigate the effects of varying the device physical parameters (7 parameters in this work) on device performance.

APPROACH

The approach to HBT optimization can be summarized as follows (and is shown in Fig. 1):

1) The intrinsic small-signal characteristics for each device profile are simulated using a two-dimensional physical model.

2) The equivalent circuit model parameters are extracted from each simulation.

3) The processing related parasitics are added to the equivalent circuit model

4) The experimental response (or goal) is formulated as a function of the device physical parameters using Taguchi's designed experiment.

The optimum design of the device high-frequency maximum available gain (*Gmax* at 10GHz) is derived through a linear regression analysis of the input parameters for all the simulations.

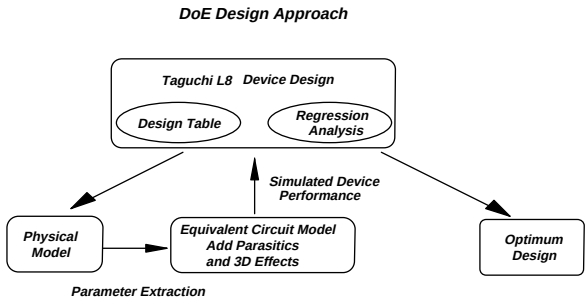

Fig. 1. The flow chart of the closed-loop design approach for the HBT profile optimization. The optimum design is derived through a linear regression analysis of the input parameters for eight experiments.

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To systematically study the effects of the device parameters on high-frequency performance, a Taguchi L8 orthogonal array *DoE* analysis has been performed, varying the base doping (N_b), base thickness (W_b), emitter doping (N_e), collector doping (N_c), collector thickness (W_c), emitter width (S_e), and base width (S_b), as shown in Table I. The design goal is to maximize the maximum stable/available gain (*Gmax*) at 10 GHz at a collector current density of 1.5×10^4A/cm^2.

TABLE I - THE DEVICE PHYSICAL PARAMETERS FOR THE DESIGNED EXPERIMENT.

#	Nb (10^{19}) (cm^{-3})	W_b (nm)	N_c (10^{16}) (cm^{-3})	W_c (μm)	N_e (10^{17}) (cm^{-3})	S_e (μm)	S_b (μm)
1	5	60	1	1.5	1	2	2
2	5	60	1	0.5	10	4	4
3	5	120	10	1.5	1	4	4
4	5	120	10	0.5	10	2	2
5	1	60	10	1.5	10	2	4
6	1	60	10	0.5	1	4	2
7	1	120	1	1.5	10	4	2
8	1	120	1	0.5	1	2	4

The *DoE* analysis is performed using a combination of (1) an accurate two-dimensional drift-diffusion based physical model [1] and (2) an automated parameter extraction technique for direct extraction of the element values of a hybrid-p equivalent circuit model from measured *S*-parameters [2]. Both of these modeling techniques have been previously shown to accurately match the M/A-COM HBT performance [1,2]. The accuracy of the model is shown in Fig. 2, a comparison of the modeled (combined physical and equivalent circuit - see Approach above) and measured *Gmax* for a two-finger 3 $\times$10 μm^2 profile I HBT at 3V and 7.2mA.

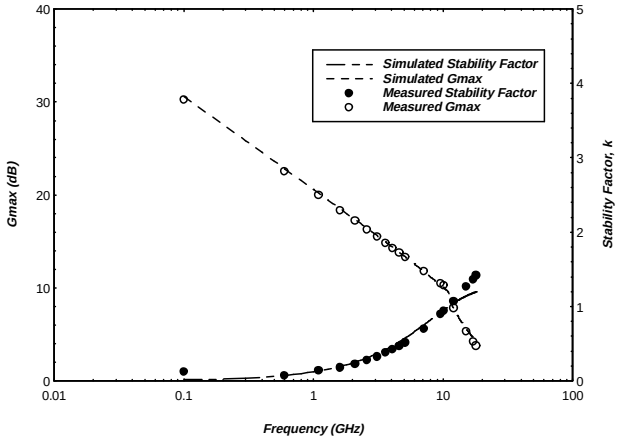

Fig. 2 The measured and simulated (using a combination of the physical and equivalent circuit model) *Gmax* and *k* for a two-finger 3×10 μm^2 HBT at 3V and 7.2mA.

RESULTS AND DISCUSSION

A. DoE Analysis

Using the gain as the experiment goal, a linear regression model has been fit to the eight experiments (Table I) to obtain an analytical expression for the device gain (*Gmax* at 10 GHz and collector current density of 1.5×10^4 A/cm^2) as a function of the input parameters. Table II lists the *DoE* predicted and the measured results for M/A-COM's baseline profiles I and II. In both cases, the predicted gain is within the process standard deviation, indicating the accuracy of the *DoE* model.

TABLE II - *DOE*-PREDICTED AND THE MEASURED *GMAX* AT 10 GHZ, 3V AND 7.2MA FOR M/A-COM'S BASELINE PROFILES I AND II.

HBT PROFILE	MEASURED		DOE
	Mean	*Std. Dev.*	
I	10.6	0.2	10.9
II	12.6	0.5	13.1

Figure 3 gives the *DoE* analysis of the relative change in *Gmax* at 10 GHz to device parameters from Table I. The *DoE* results highlight some interesting trends for the design of the device doping profile.

First, over the range of parameters considered, the highest possible base doping should be used. This lowers the base resistance and improves *Gmax*. The limitation of the base doping comes primarily from heavy doping effects, including the reduction of minority carrier mobility in the base, which results in a reduced f_t (and thus a reduced f_{max}). The *DoE* analysis demonstrates that for the doping ranges considered, the reduction in f_t is more than offset by the reduced base resistance.

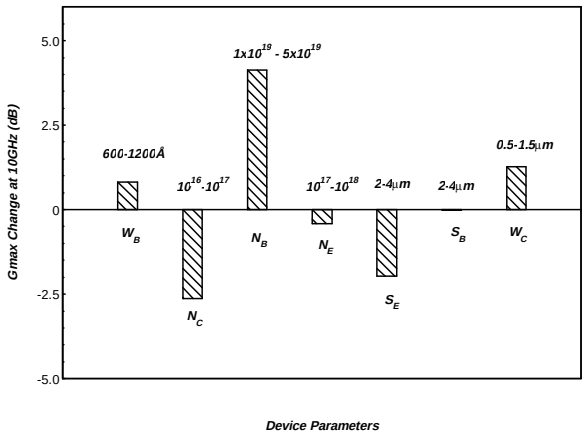

Fig. 3 The *DoE* predicted relative change in *Gmax* at 10 GHz due to variations in device parameters. For example, as the collector doping is increased from 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3}, *Gmax* drops by approximately 2.5dB.

Second, for a given base doping, the base should be made thicker to reduce the base resistance and improve the gain. Again, the *DoE* analysis shows that up to a 120nm base thickness, the reduction in base resistance resulting from a thicker base more than offsets the reduction in f_t from a thick base.

Third, the collector should be made as thick as possible in order to obtain the maximum undercut of the extrinsic base-collector capacitance, provided that the etching rate and profile can be repeatably and precisely controlled. Finally, as expected, the high-frequency gain can be effectively improved by reducing the emitter stripe width, S_e. The tradeoff in this case, however, is increased processing complexity.

B. Design Validation

Based on the discussion in previous section, a new optimized device profile was designed with a higher base doping, lower collector doping, and thicker collector layer with no geometric dimension changes (such as the emitter stripe width). Since this optimized device contains no geometrical changes, it can be fabricated using the standard baseline process. The comparison of the measured performance between the new designed profile and baseline profile for a two-finger 3×10 μm^2 HBT at 3V and 7.2mA is shown in Fig. 4. Over 4 dB improvement in *Gmax* at 10 GHz is obtained without resorting to reduced device dimensions and/or a thin base layer.

In addition to the optimal design, three different HBT profiles have been fabricated using the baseline profile to experimentally validate the *DoE* approach. The designed (modeled) and measured performance is given in Table III; once again, the *DoE* predicted results can provide good quantitative predictions of gain with less than 0.5dB error (within the process standard deviation). Further, the modeled and measured effect of the parameters on device performance is plotted in Fig. 5, which demonstrates that, in most cases, the *DoE* approach can **quantitatively** predict the effects of parameter variations. The discrepancy in N_c is likely due to confounding and can be removed by resorting to higher level designs with more

experiments. In effect, the analysis has allowed for the development of device design rules which can be easily used to quantitatively predict the effects of material profile and device geometry changes on performance.

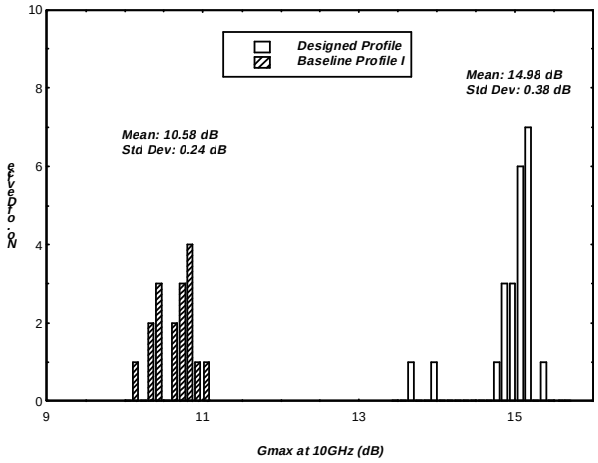

Fig. 4. Measured comparison of the new profile and baseline profile for a two-finger 3×10 μm^2 HBT at 3V and 7.2mA. The new design achieves over 4 dB improvement in *Gmax* at 10 GHz without resorting to reduced device dimensions and/or a thin base layer

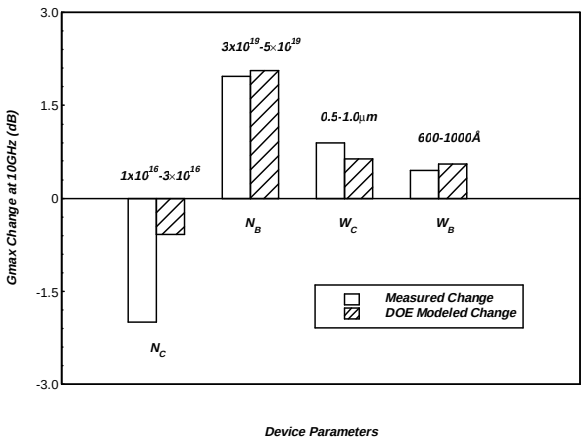

Fig. 5. Comparison of the modeled and measured relative change in *Gmax* at 10 GHz due to variations in device parameters. In most cases, the *DoE* approach can quantitatively predict the effects of parameter variations. The discrepancy in N_c is likely due to confounding (as discussed in the text).

TABLE III. THE DESIGNED (MODELED) AND THE MEASURED PERFORMANCE OF THREE NEW PROFILES.

		MEASURED		DOE
PROFILE	*No. of Dev.*	*Mean*	*Std. Dev.*	
III	54	13.0	0.3	13.6
IV	27	12.1	0.5	13.0
V	54	15.0	0.4	14.2

CONCLUSION

A closed-loop design approach is developed by combining physical modeling and equivalent circuit modeling. *DoE* analysis is used to quantitatively investigate the effects of varying the device physical parameters on device high-frequency performance. The technique provides a very efficient method and powerful tool for device design and profile optimization, and was applied to the high-frequency optimization of the M/A-COM HBT, yielding a 4 dB gain improvement at 10GHz over the baseline process - without resorting to reduced dimensions.

REFERENCES

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[2] G. N. Henderson, *Intl. Journal of MMWCAE*, vol. 6, pp. 153, 1996.

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